What is claimed is:

1. An electrically rewritable nonvolatile semiconductor memory device comprising:

a plurality of memory circuits, each of which has a control circuit for sequentially controlling writing, provided in a memory chip so as to share a data bus, and

a chip enable terminal for controlling the activity and inactivity of each of the memory circuits provided for each of the memory circuits.

2. The nonvolatile semiconductor memory device as set forth in claim 1, wherein each of said memory circuits is provided with a ready/busy signal terminal which corresponds to said chip enable terminal.

3. The nonvolatile semiconductor memory device as set forth in claim 2, wherein a master chip enable terminal for controlling the activity and inactivity of said plurality of memory circuits as a whole, and the activity and inactivity of each of said memory circuits are controlled by a logical output of a signal of said master chip enable terminal and a signal of said chip enable terminal of each of said memory circuits.

4. The nonvolatile semiconductor memory device as set forth in claim 3, wherein said logical output is an output of an AND gate where the signal of said master chip enable terminal and the signal of the each chip enable terminal are applied.

5. An electrically rewritable nonvolatile semiconductor memory device having a plurality of memory circuits, each of which has a control circuit for sequentially controlling writing, provided in a memory chip so as to share a data bus,

wherein the activity and inactivity of each of the memory circuits are controlled by inputting a command.

6. The nonvolatile semiconductor memory device as set forth in claim 5, wherein a common chip enable terminal is provided

for said plurality of memory circuits, and an enable signal inputted to said chip enable terminal is supplied to a selected one of said memory circuits which has been selected by inputting said command.

7. The nonvolatile semiconductor memory device as set forth in claim 6, wherein two of memory circuits are alternatively made enable by said command.

8. The nonvolatile semiconductor memory device as set forth in claim 6, wherein a common ready/busy signal terminal is provided for said plurality of memory circuits, and a ready/busy state of said selected one of said memory circuits, which has been selected by inputting said command, is outputted to said ready/busy signal terminal.

9. An electrically rewritable nonvolatile semiconductor memory device wherein a plurality of memory circuits, which are able to assign an address, are provided in a memory chip, and each of said memory circuits is provided with at least one stage of data buffer for transmitting writing data corresponding to said address, and wherein writing operations in said plurality of memory circuits are simultaneously carried out via said data buffer.

10. The nonvolatile semiconductor memory device as set forth in claim 9, wherein a pass/fail result of each of writing operations is outputted to each of said memory circuits.

11. The nonvolatile semiconductor memory device as set forth in claim 10, wherein said pass/fail result is outputted every memory cell.

12. The nonvolatile semiconductor memory device as set forth in claim 10, wherein said pass/fail result is accumulated to be held.

13. The nonvolatile semiconductor memory device as set forth in claim 10, which has a mode in which it is determined whether data are able to be inputted to said data buffer by referring to said pass fail result, and a mode in which it is determined whether data are able to be inputted to said data buffer without referring to said pass/fail result.

14. The nonvolatile semiconductor memory device as set forth in claim 11, which has a mode in which it is determined whether data are able to be inputted to said data buffer by referring to said pass fail result, and a mode in which it is determined whether data are able to be inputted to said data buffer without referring to said pass/fail result.